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Ultra-Fast All-Optical Logic Circuit With The Massive Use of Non-Linear Material

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Abstract: Nonlinear material based all-optical switching mechanism is used here to develop the all-optical logic operation scheme. A single bit logic unit has been accessed first and is elevated to a higher bit logic unit in course. These circuits can execute innumerable logic operations and remarkably, they are all-optical and fully parallel in nature. These all-optical logic units can gear up to the highest capability of optical performance in high-speed all-optical computers.

Keywords: Nonlinear material, optical switching, all-optical NOT gate, multi-output gate, multiplexing circuit, logic circuit

I. INTRODUCTION

No day can be imagined today without the talismanic touch of computer. In the coming future, we are to face rising usage of the Internet along with more complex and sophisticated problems in different walks of life, as computer is widening its globe. It compels us to think of such a computer which is not only faster but also more reliable. Unfortunately, the VLSI technology, so far is being used in electronics, is already in a saturated state from both the aspects – size and speed. To deal with the soaring demands, optics has already established its validity in various arithmetic [1-6], logic [7-13], algebraic [14-18], and image operations [19-22] in last few years, preliminary because of its promising features of parallel, high speed, high bandwidth non-interfering communications [5, 7, 9-11, 19, 23-24]. These gifted advantages lead us to our dream goal of making the fastest possible computer, specifically, a super fast optical computer that will outperform the fastest possible electronic computer.

Different techniques have been proposed and developed to implement several components of super fast computer in optical domain. In the recent past, all-optical switching mechanism [5, 9-13, 25-27, 29, 34] by nonlinear optical material is well-known as one of such promising techniques. Arithmetic operations as well as logical operation are the two essential tasks in any type of computing system. The Arithmetic operation scheme [6] has been proposed earlier. This paper proposes a scheme for the all-optical implementation of logic operational circuit with proper use of nonlinear material-based all-optical switching mechanism. At first, we design an all-optical gate (Multi-output gate) which can give three distinct logic outputs of the very same inputs at the same time. Then, an all-optical multiplexture is designed. Finally, we combine these two circuits to develop a single bit logic operation scheme. As the circuit is purely all-optical in nature, it is very simple and very fast. All the basic logic operations and XOR operation can be achieved with extreme accuracy. The scheme can be extended to a higher bit logic operation scheme easily. An ALU of the proposed goal, an optical computer, can be implemented through this scheme.

II. ULTRA-HIGH-SPEED ALL-OPTICAL SWITCHING BEHAVIOR OF NONLINEAR MATERIAL AND ITS USES AS ALL-OPTICAL NOT GATE, MULTI-OUTPUT GATE AND AND GATE

The phenomenon photorefractivity [10-12, 28] of some nonlinear optical material is used in nonlinear all-optical intensity switching mechanism. The refractive index [10-12, 20, 28, 30-31] of some nonlinear materials (NLM) such as carbon disulfide, pure silica, potassium dihydrophosphate (KH_2PO_4 (KDP) crystal etc. varies linearly with the intensity of the light incident on it. The refractive index (n) of such isotropic dielectric non-crystalline media can be put into an equation as (1). Here n_0 is the linear term, n_1 is the nonlinear correction term and I is the intensity of the incident light beam on the material.

$$n = n_0 + n_1 I$$

A. Ultra Fast All-Optical Switching Behavior of Nonlinear Material

We can implement the switching mechanism with such nonlinear material by taking an interface between two media of which one is a linear material (LM), whose refractive index n_0 is independent of the intensity of light and the other is aforesaid NLM. A laser beam, highly intense polarized light, preferably pulse laser of intensity $I_{1,}$ is allowed to incident on the interface from linear to nonlinear part in a particular direction XO (incidence angle θ_1) as it depicted in Fig. 1. The refracted beam from the NLM follows the path OZ. But when another higher intense laser beam of intensity I_2 ($I_2 > I_1$) is made to incident along XO, after refraction from the NLM the light passes through OY direction (angle of refraction θ_2). The deviation of refractive angle for different incident light intensity I_1 and I_2 is $\angle ZOY = \Delta\theta_2$. Thus the combination of LM and NLM may act nicely as a directional all-optical switch. This is the unit block of our proposed logic circuit.

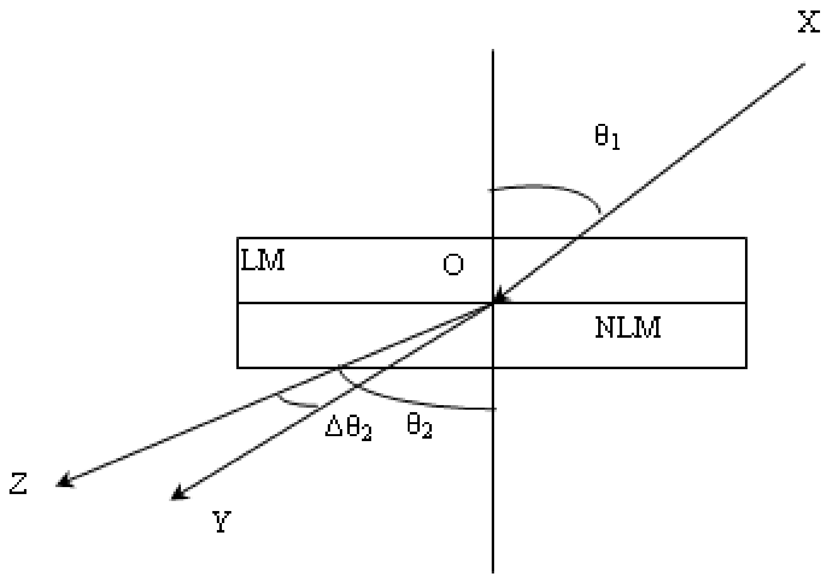


Figure 1: Intensity switching of optical nonlinear material

In the expression of refractive index in Eq. (1) n_0 is linear term and n_1 is the nonlinear correction term. For carbon disulfide [10-12, 29] (CS_2) $n_0 = 1.63$, $n_1 = 514\times10^{-20}$ m^2/W. and for fused silicon dioxide [10-12, 29] (SiO_2) $n_0 = 1.458$, $n_1 = 2.7\times10^{-20}$ m^2/W. If we use CS_2 and SiO_2 as nonlinear materials and the pulse laser of intensity I = 2×10^{18} W/m^2 as a source, we can estimate the deviations of light in two cases as given in Table I.

Table I. Estimation of the deviation of pulsed laser light when passing through carbon disulfide (CS_2) and silicon dioxide (SiO_2)

Material	***Angle of incidence (θ_1)***	***Incident light intensity***	***n (= $n_0 + n_1 I$)***	***Angle of refraction (θ_2)***	***Deviation ($\Delta\theta_2 = \theta'_2 - \theta''_2$)***
Carbon disulfide (CS_2)	45 deg	I=2×10^{18} W/m^2	11.91	3.404 deg = θ'_2	1.578 deg
	45 deg	2I	22.19	1.827 deg = θ''_2	
silicon di-oxide (SiO_2)	45 deg	I=2×10^{18} W/m^2	1.512	27.883 deg = θ'_2	1.041 deg
	45 deg	2I	1.566	27.842 deg = θ''_2	

The logic gates [10-12, 28-29] are implemented in optics using NLM by taking the presence of light signal as 1 and the absence of it as 0.

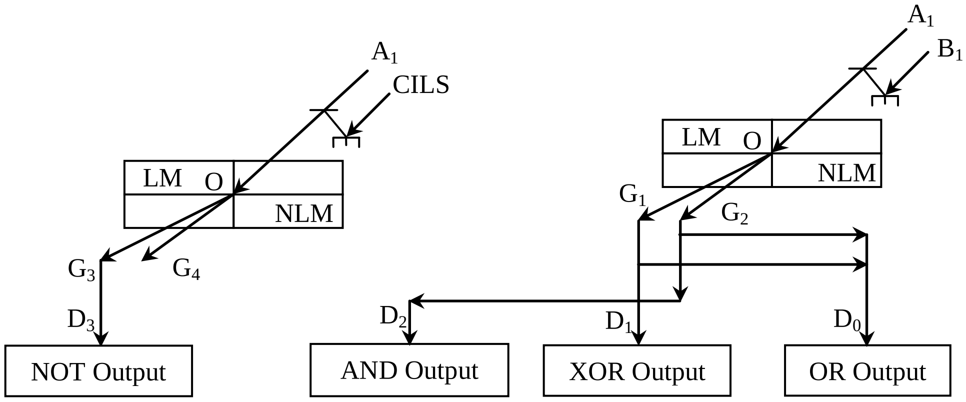
The implementation of such logic gates can be done by using some femtosecond laser pulses and 1-mm-thick KDP crystal at the pick intensity of 0.6 TW/cm^2 and duration of 60 fs [10-12, 29]. M. Choi et al. show that a single-layer terahertz metamaterial [31] has a peak refractive index of 38.6 while maintaining low losses. It is a broadband, extremely high index of refraction going beyond the limit that is attainable with naturally existing substances, lead sulphide, and strontium titanate [31].

B. All Optical **NOT** *Gate*

To implement an all-optical NOT gate using non-linear material, a constant intensity pulse laser source (CILS) is used as shown in Fig. 2(a). It is also called probe beam. Here A_1 is taken as input beam. A detector is placed at D_3 will detect the output beam after refraction. If A_1 is absent, the light will follow a path OG_3 and will be detected by the detector due to presence of CILS. But if A_1 is present, after refraction, the light will follow a path other than OG_3, may be OG_4, and the detector will not detect any light signal. So D_3 is equals to $\overline{A_1}$. Thus the system (NG block) acts as all-optical NOT gate.

C. All Optical Multi-Output Gate

We design an all-optical Multi-output gate which can give three different logic outputs of same inputs at the same time, shown in Fig 2(b). Here A_1 and B_1 are two input channels. Three detectors placed at D_0, D_1 and D_2 give the outputs. If any one of the input signals carries light, after refraction light will follow the path OG_1. The path OG_2 will carry light if both A_1 and B_1 are present.



(a) **(b)**

Figure 2: All-optical logic gates (a) NOT gate (b) Multi-Output gate

Now, we direct light from both the path OG_1 and OG_2 to D_0 detector. When both the channels remain dark, D_0 gives 0, otherwise it is 1. So, at D_0, we get simply logical OR Output of A_1 and A_2 inputs, i.e. $D_0 = A_1 \vee A_2$. If only one input carries light, the light ray after refraction will be detected by the detector at D_1, otherwise not. Thus, D_1 gives ($A_1 \oplus A_2$) output. Now when both the channels carry light signal, the light beam after passing through the block will be detected by the detector at D_2, otherwise not. Hence one can get AND output of the inputs A_1 and A_2 at D_2 terminal ($D_2 = A_1 \wedge A_2$). So the block MG simultaneously acts as OR, XOR and AND gates (We would like to define it as Multi-output (MG) gate).

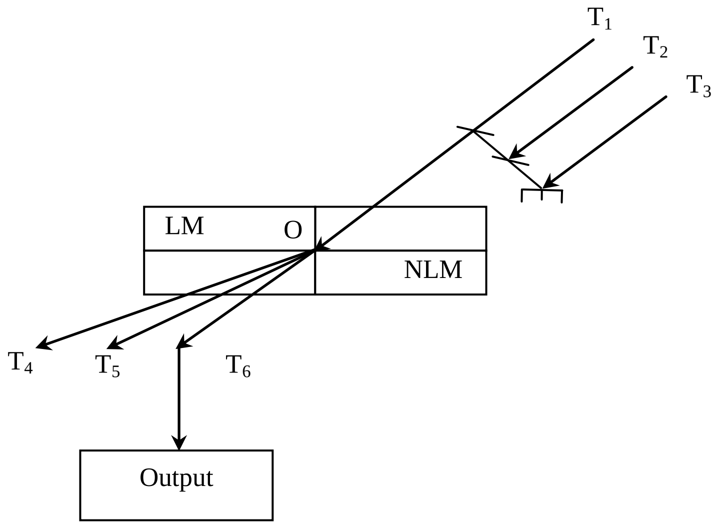


Figure 3: All-optical three input AND gate

D. *All Optical* AND *Gate*

The Three-input-all-optical AND gate using NLM is shown in Fig 3. Here T_1, T_2 and T_3 are the three input channels. Light can travel through any of the three paths OT_4, OT_5, OT_6. A detector placed at T_6 gives the output. Now when all the channels carry light signal, the light beam after refraction will be detected by the detector at T_6, otherwise not.

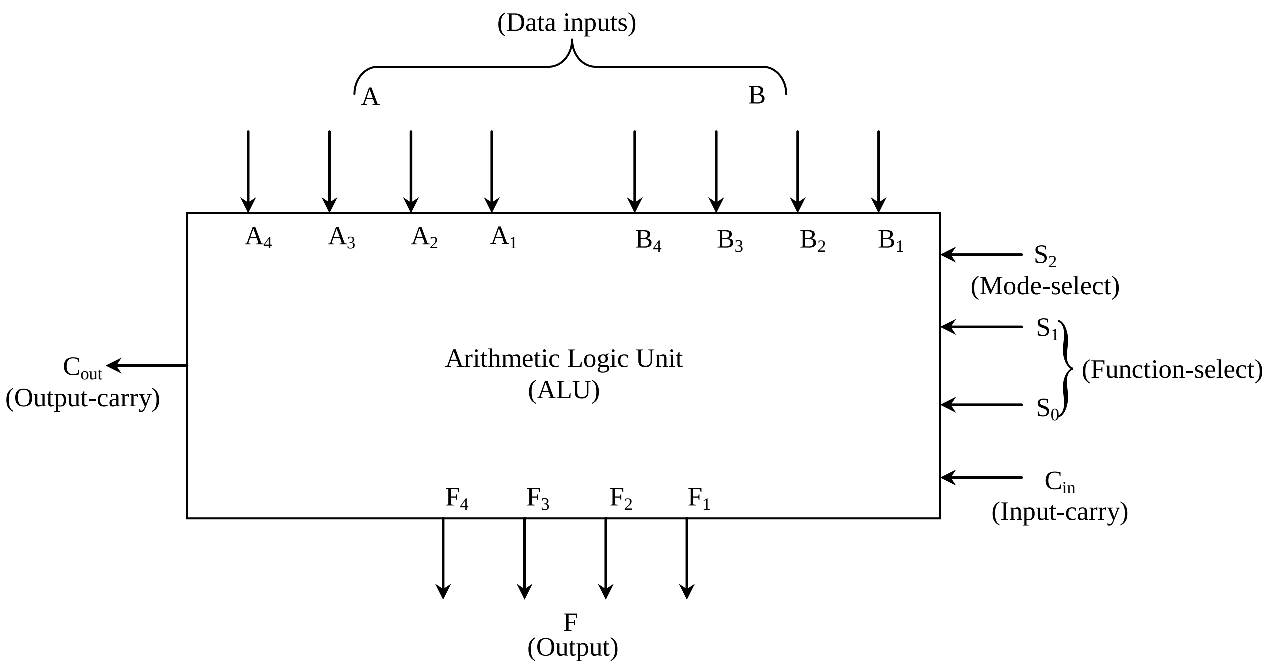


Figure 4: Block diagram of a conventional four-bit ALU

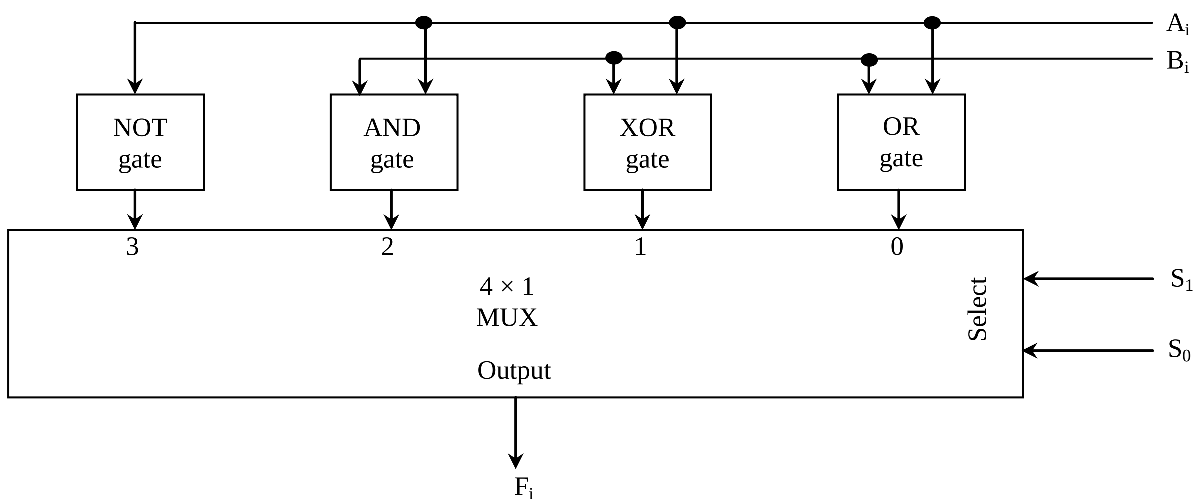


Figure 5: Electronically addressed one bit (ith stage) logic circuit

III. CONVENTIONAL ELECTRONIC LOGIC CIRCUIT IN ALU

The block diagram of a 4-bit conventional ALU [32-33] is shown in Fig. 4. If $S_2 = 1$ ALU acts as logic unit, Input-Carry (C_{in}) and Output-Carry (C_{out}) have no meaning. The simplest conventional electronic logic circuit is shown in Fig. 5 which depicts one typical stage designated by subscript i. It can be repeated n times for an n-bit logic circuit. The output of four logic gates, OR, XOR, AND and NOT respectively, are the data inputs of a 4×1 MUX. The output F_i is one of the four logic operations according to the proper combination of function-select inputs, S_1 and S_0. The function table is shown in Table II.

Table II. Function table for the all-optical logic circuit

Function-selection variables		***Output equals to***	***Circuit action***
S_1	***S_0***		
0	0	$F_i = A_i \vee B_i$	OR Operation
0	1	$F_i = A_i \oplus B_i$	XOR Operation
1	0	$F_i = A_i \wedge B_i$	AND Operation
1	1	$F_i = \overline{A_i}$	NOT Operation

IV. CONCEPT OF MULTIPLEXING

Multiplexing is nothing but transmitting a large number of information units over a lesser number of outlines [5, 32-33]. It is also named as data selector, because it selects one of many inputs and guides the binary information to the output channel. The digital multiplexer is a combinational circuit that selects binary information from one of several input lines and directs it to a single output channel. The choice of a particular input line is restricted by a set of selection input lines. Normally, there is 2^n input channels and the bit combinations of n selection inputs determine that very input which is selected. The block diagram of a 4-line to 1-line multiplexer (4×1 MUX) is shown in Fig. 6(a). Each of the four data input lines, D_0 to D_3, is selected and sent to the output Y by the proper combination of select inputs S_1 and S_0. The function table is shown in Table III.

Table III. Function table for of 4×1 multiplexture circuit

select inputs		***Output Y equals to***
S_1	***S_0***	
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

V. ALL-OPTICAL MULTIPLEXING SYSTEM

The scheme of all-optical multiplexer [25, 32-33] is made of with the combinational blocks of linear and nonlinear materials shown in Fig. 6(b). Here NG1 and NG2 are two all-optical NOT gates and AG1 to AG4 are four three input AND gates. The input lines S_1 and S_0 act as select inputs of the data selector. D_0, D_1, D_2 and D_3 are the four data input lines and Y is the final output of the MUX.

Here S_0, is the input of NG1 and S_1 is the input of NG2.CILS1 and CILS2 are the two probe beams of the two NOT gates NG1 and NG2 respectively. As NG1 and NG2 are two NOT gates, S_0 and S_1 are inverted through O_1C_1 and O_2C_2 paths respectively and they are represented as S'_0 and S'_1. We take the direct input S_0 and also the complement of S_0 (S'_0) as two outputs from NG1. Similarly, from NG2, S_1 and S'_1 are in use.

Now, AG1, the first AND gate, has inputs D_0, S'_0 and S'_1 and here we pick up the output N_3 solely. The first data input, D_0 is transferred to the output Y through AG1 if and only if S'_0 and S'_1 are both at high state (i.e. $S_0S_1 = 00$). In this situation exclusively the block AG1 will be active but not the other blocks AG2, AG3 and AG4. Secondly D_1, S_0 and S'_1 are the inputs of AG2 block and here the output is taken from N_4 terminal. At the third AND gate, AG3 gets inputs from D_2, S'_0 and S_1 and the output is received from N_5 end. D_3, S_0 and S_1 are taken as the three inputs of AG4 and here N_6 channel yields the output. Similar to the first case at AG1, the data at D_1, D_2 and D_3 are transferred to the output Y respectively if and only if other two inputs of each AND gates are at logical '1' stage. Ultimately, all the outputs (N_3, N_4, N_5 and N_6) of four AND gates are united to form the ultimate output Y of the 4×1 MUX.

Now, we need to explain the operation of the multiplexer referred to Fig. 6(b). Let us take the select input $S_0 = S_1 = 0$ (i.e. S_0 and S_1 both remain dark). Due to presence of probe beams CILS1 and CILS2, light signal will follow the path O_1C_1 and O_2C_2 when passing through the block NG1 and NG2 respectively. At present, we have $S_0 = S_1 = 0$ and $S'_0 = S'_1 = 1$. In this condition, the first AND gate (AG1) is active to transfer output through O_3N_3 to Y. We can get light at Y (=1) when $D_0 = 1$, and we will not have it when $D_0 = 0$. In the present situation, all other AND gates will stay inactive, because either one or both of the control inputs S_0 and S_1 have no light. So, N_4, N_5 and N_6 terminals have no light signal whatever may be the status of D_1, D_2 and D_3 lines. Thus, we come to the decision that only the data input D_0 is connected to the output channel Y in absence of S_0 and S_1. Similarly, if $S_0 = 1$ and $S_1 = 0$, only the AG2 gate will be active and none other than D_1 is connected to Y. In the same manner, when $S_0 = 0$ and $S_1 = 1$, only the D_2 channel will remain connected to Y, and when $S_0 = S_1 = 1$, only D_3 will be connected to the final output.

VI. ALL-OPTICAL LOGIC CIRCUIT

We now propose a simplest all-optical logic operation scheme which is illustrated in Fig. 7. This picture expresses one typical stage chosen by subscript i. It can be repeated n times to obtain an n-bit logic circuit. The output of four logic gates, OR, XOR, AND and NOT respectively, are the data inputs of a 4×1 MUX. According to the proper combination of function-select inputs, S_1 and S_0, the output F_i is one of the four logic operations. The function table is shown in Table II.

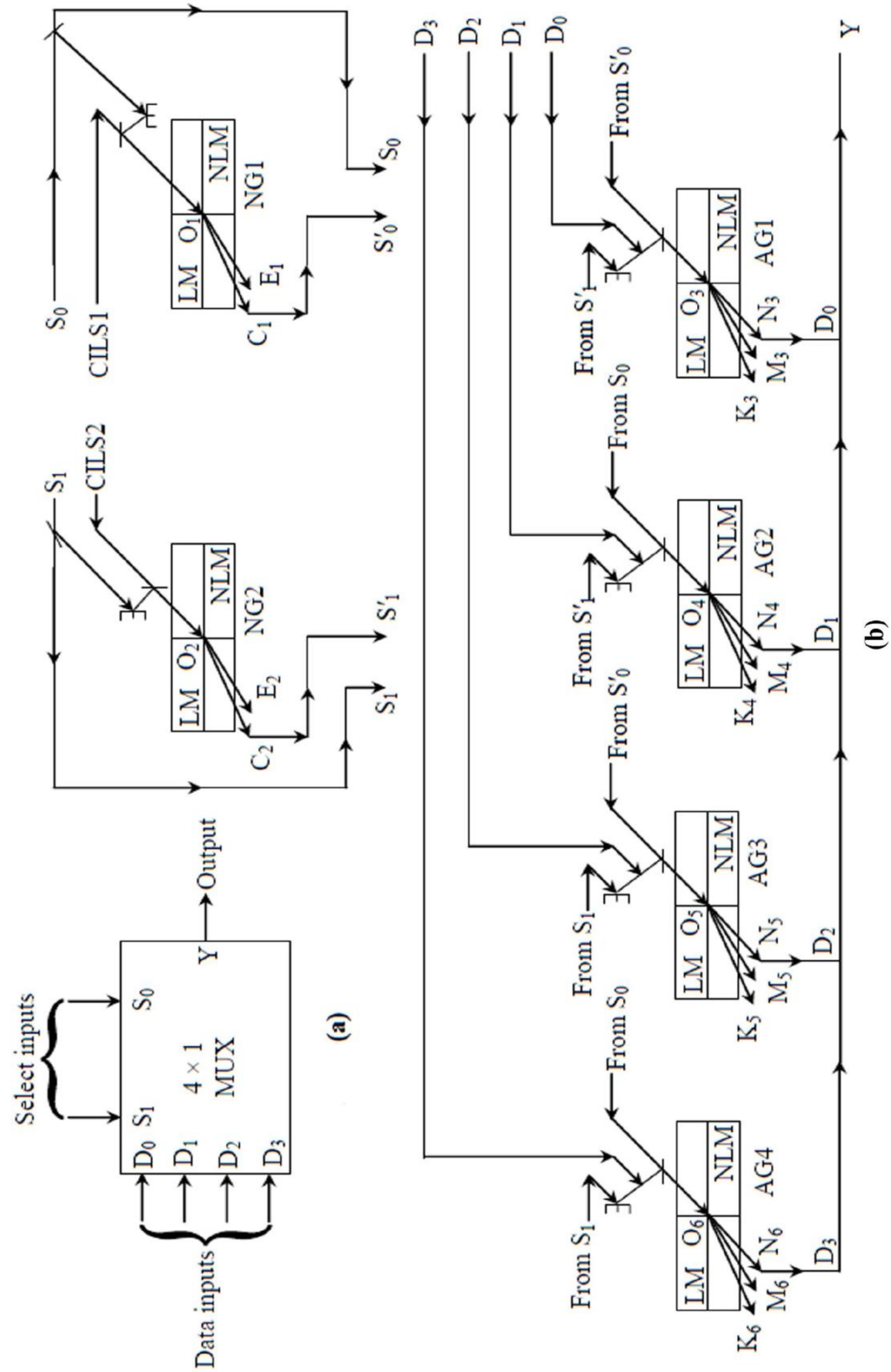


Figure 5: Multiplexer (a) Block diagram of a conventional 4-line to 1-line multiplexer (b) All-optical multiplexer circuit.

Here A_i and B_i are the two one bit (i^{th} bit of an n bit binary numbers) binary numbers used as data inputs of our scheme which are combined with each other to generate a logic operation at F_i output. The two selection variables, S_1 and S_0, specify the particular logic operation to be produced at the final output channel F_i. It is possible to create a total four logic operations (OR, XOR, AND and NOT) by the combination of two control bits S_1 and S_0. The circuit is constructed by eight blocks (combinations of linear and nonlinear materials), our unit blocks. Among eight unit blocks, NG1, NG2 and NG3 are the three NOT gates, AG1, AG2, AG3 and AG4 are the four three input AND gates and MG is a Multi-output gate.

To explain it more legibly, let us divide the circuit into two parts.

Part I: Logic Operation Part: The Logic Operation Part is enclosed by the doted rectangle in Fig. 7. The blocks, MG and NG3, form the first part. A_i and B_i are inputs to MG, the Multi-output gate. The three outputs from it are D_0 (=$A_i \vee B_i$), D_1 (=$A_i \oplus B_i$), D_2 (=$A_i \wedge B_i$). The NOT gate has input A_i along with the probe beam CILS. One can expect the output of NG3, $D_3 = \overline{A_i}$.

Part II: 4×1 Multiplexer Part: The rest part of Fig. 7 other than the Logic Operation Part is 4×1 Multiplexer Part. Two NOT gates, NG1 and NG2, and four AND gates, AG1, AG2, AG3 and AG4, construct the multiplexer part of the logic circuit. The select variables S_1 and S_0 are inverted by NG2 and NG1 respectively. The combination of two variables (S'_0, S'_1 for AG1; S_0, S'_1 for AG2; S'_0, S_1 for AG3 and S_0, S_1 for AG4) is used in the said manner as two inputs of the four three inputs AND gates. The outputs from Logic Operation Part, D_0, D_1, D_2 and D_3, are third inputs of each AND gates AG1 to AG4 respectively.

Now four cases may arise

Case 1: When $S_1 = S_0 = 0$, then $S'_1 = S'_0 = 1$, that activates none other than the first AND gate AG1. As a result, only D_0 (=$A_i \vee B_i$) is transferred to the final output F_i through O_3N_3 and Y_0. In this situation, other three AND gates (AG2, AG3 and AG4) remain inactive, independent to the input variables. Thus we can conclude that the logic operation scheme produces the final output $F_i = A_i \vee B_i$ when S_0 and S_1 both at logical '0' state. In other words, we can say that the circuit performs the OR logic operation for $S_1S_0 = 00$.

Case 2: Now when S_0 (= 1) carries light but S_1 (= 0) does not, we have $S'_1 = 1$ and $S'_0 = 0$. This turns the second AND gate, AG2 active but not the other three AND gates. As an outcome F_i is nothing but D_1 (=$A_i \oplus B_i$). The circuit gives EX-OR operation when $S_1 = 0$, $S_0 = 1$.

Case 3: Next, when S_0 is dark but S_1 is lighted, i.e. $S_1 = 1$ and $S_0 =0$, then $S'_1 = 0$ and $S'_0 = 1$. As S_1 and S'_0 both carry light signal, AG3 becomes active but not AG4, AG2 and AG1. Only the D_2 (=$A_i \wedge B_i$) terminal is supposed to be connected to F_i via O_5N_5 and Y_2. The ultimate result of our scheme, F_i generates AND operation of the data inputs A_i and B_i if and only if S_1 is equal to 1 and S_0 is equal to 0.

Case 4: In the penultimate condition, when both the select bits S_0 and S_1 are present ($S_1 = S_0 = 1$), there will be on light at S'_1 and S'_0 ends. Now, the fourth AND gate (AG4)

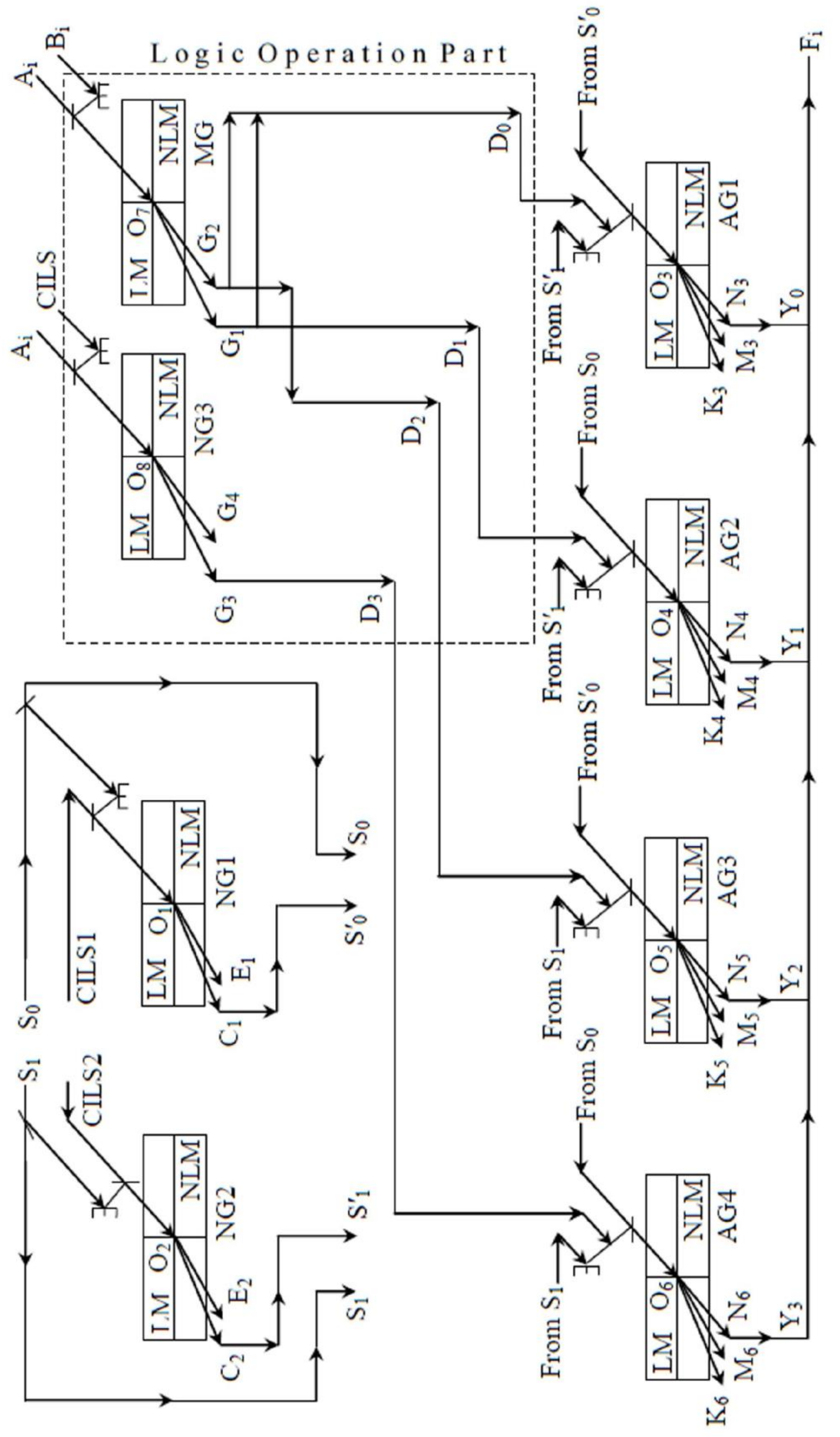


Figure 7: All-optical one bit (i^{th} stage) logic circuit.

shifts D_3 (= $\overline{A_i}$) output to F_i through O_6N_6. All the other AND gates are inactive now, since either one or both of the control inputs S'_0 and S'_1 have no light. Thus we come to the decision that in presence of S_0 and S_1 (i.e. S_1S_0 = 11) only the NOT operation of A_i is executed by the logic circuit.

VI. CONCLUSION

The proposed technique of all-optical implementation of logic operation scheme is very fast (above THz) as it is fully all-optical. The light signals that are severally used, bended and the feedback light signals from the outputs are made by mirrors and beam splitters to make the circuits simple. This operation scheme should be the second step on our dream way to all-optical Arithmetic and Logic Unit. Along with this the circuit being parallel becomes remarkably fast. Proper findings of nonlinear material may be a significant issue here. Essentially inputs should be chosen properly for proper function of the system.

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