Design and Simulation of I2C Master Core

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Abstract: The design module of I2C master core is presented in this paper. I2C is a bi-directional serial bus including collision detection and arbitration that is used for exchanging the data between various integrated circuits or devices. I2C is best for short distance communication between many devices. It uses SDA and SCL lines to exchange data. The design module is implemented on Xilinx project navigator using Verilog HDL. Verification of this design module is done using test benches created to check the functional correctness prior to its fabrication. Numbers of seeds are used to generate different random numbers to run the same test case.

Keywords: I2C, Slave, DUT, Seed, Master

I. INTRODUCTION

The benefits of serial communication outweigh parallel communication in terms of less connections on printed circuit boards with less requirement of wiring. Many applications of embedded system such as A/D converter, D/A converter, sensors for temperature use serial communication. The processor performs the operation without need of memory in serial communication. The protocols such as RS-232, SPI, UART, RS-422, CAN, USB are used to interface devices under low and high-speed conditions. But, the major disadvantage of these protocols is requirement too many connections to perform the operation. Phillips came with a protocol named I2C [1-3] to overcome this problem which needs only two pin connections.

In this paper, an I2C master core is designed that provides a simple and efficient method to exchange data between various devices using Verilog HDL. System Verilog is a combination of HVL (hardware verification language) and HDL (hardware description language). System Verilog has its own assertion specification language, which is used for verification of the design. Randomization is also included in this language and every random value is checked through this process. The design module a multi - master bus. This system consists of 2 bus lines, SDA and SCL, serial data and serial clock lines. Originally, it was invented for communication in TV sets. It is very simple and short distance protocol [1-6].

II. DUT – I2C MASTER CORE

DUT or design under test is the name given to the hardware model that we code using a hardware description language like Verilog HDL. Here the DUT is a I2C master core that is verified by creating an environment around it that simulates the signals given and taken from it.

The I2C master core communicates with various slaves connected to it by giving commands of write and read functions. This is how we verified the I2C core [5-6] functionality for a single slave and reset whenever needed. The Bus comprises of two active wires called Serial data line (SDA) and Serial clock line (SCL). Master Core is the one that initiates communication and Slave is the one that is addressed. The bus is checked to know its free status when an IC is requesting to communicate with

another IC and this is done by checking SDA and SCL lines. If free, start operation is generated by the Master and SCL provides clock signal as reference and address is put in serial form on SDA of each device [1-6].

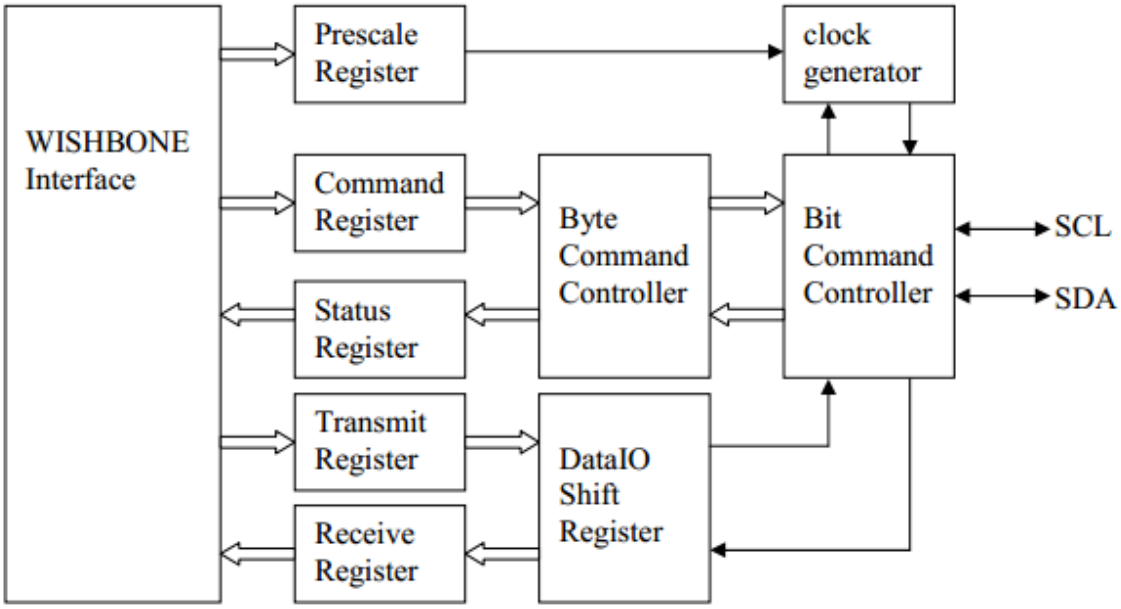


Figure 1. I2C Bus architechture [1-6]

III. OPERATIONS BY I2C

A. System Configuration

The I2C system used SDA and SCL lines for transferring data to the integrated circuits. Data is send to the slave and the master in a synchronous way to serial clock line on the serial data line on byte by byte basis. The size of each data byte is 8 bits and for each data bit there is one serial clock line pulse with the most significant bit transferred first [1-6].

B. I2C Protocol

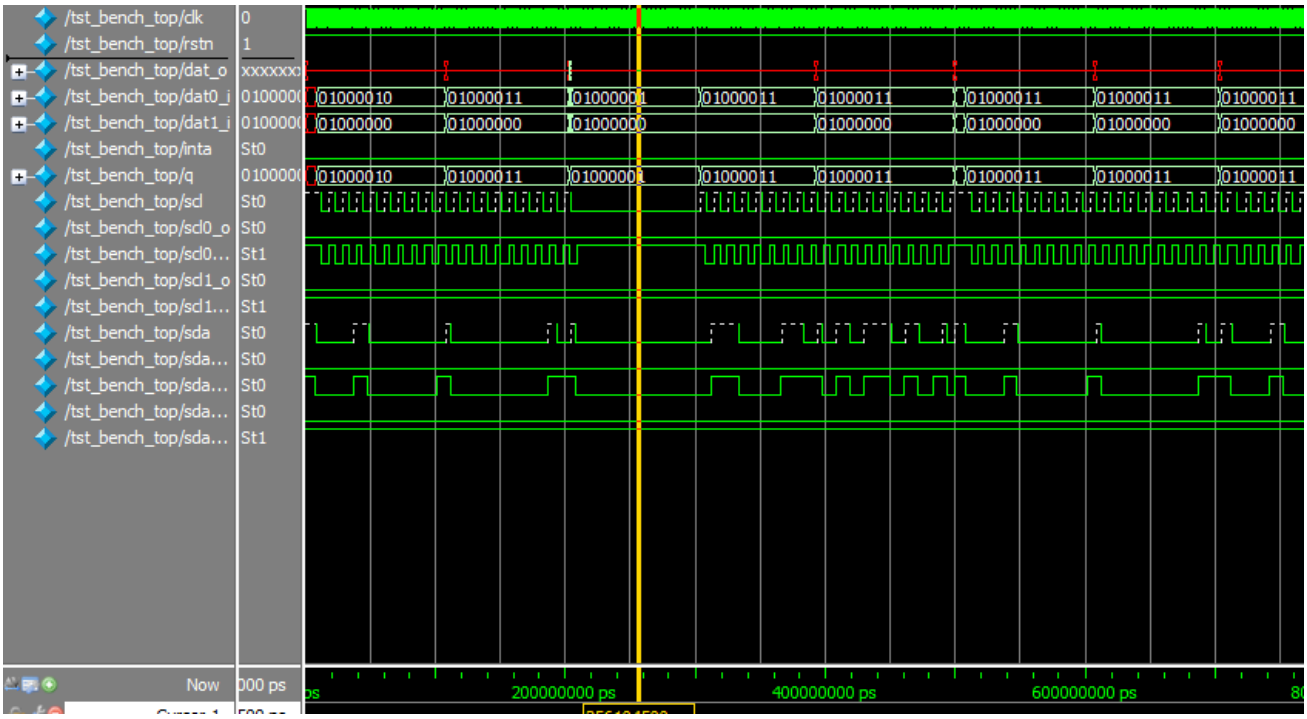
Normally, a standard communication follows four parts, that is, first the start signal generation as shown in figure 2 with the S-bit sent first, then the address of the slave is transferred with read and acknowledgment, after that the 8-bit data is transferred bit by bit and at the last the stop signal is generated as shown with the P-bit [1-6].

Figure 2. 7-bit data transfer

When the bus is free or idle, that means no other master device is using the bus, i.e., both SCL and SDA lines are high, a master initiates a transfer by sending START signal. A START signal, usually referred to as the S-bit as shown in figure 2, is defined as a high-to-low transition of serial data line (SDA) while serial clock line (SCL) is high. The S-bit which is the start signal is always generated at the beginning of a new data transfer [1-6].

IV. RESULT

I2C master was designed in Verilog HDL known as the design module on Xilinx project navigator and the test bench is made to test the design module. The designed is implemented on FPGA Nexys 6 board [4]. The test bench provides the inputs to the design module and verification of outputs is also done in the test bench. Test bench should be created in such a manner that it works in all possible conditions. Model sim was used to verify the design functioning or simulation.



V. CONCLUSIONS

This paper presents the simulation and design of I2C master core. The design is implemented on Xilinx project navigator using Verilog HDL. Verification of the module is performed using ModelSim simulation tool. The DUT we have used here is rather simple but successful verification of it can help understand the complex process of verification and open doors for further work.

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Ethical statement: The authors declare that they have followed ethical responsibilities.

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