A linear, dual-Wideband, low power CMOS LNA with current reuse and notch filter topology for UWB applications

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Abstract: A low power, ultra-wide-band (UWB) Low Noise Amplifier (LNA) with active notch filter for interference rejection in the 5-6 GHZ frequency band, is designed with technology 0.18 µm CMOS. The UWB LNA employs cascode stage incorporating the feedback structure and the current reuse topology to ensure good input matching with minimum power consumption and noise figure. To avoid desensitization of the UWB LNA, an active notch filter is integrated to suppress the interference causing by the existing narrowband standard such as wireless LANs standard (WLANS) which exceed the received ultra wideband signal power by more than 60 dB. The proposed UWB LNA achieves a high and flat gain of 16.9 dB in the low band (3-5GHZ) and 16.3 dB in the high band (6-10GHZ). The input and output reflection coefficient S11 and S22 are less than –9.8 dB and –10 dB respectively. A minimum noise figure which is within the 2.3-3.2 dB. The input referred third-order intercept point (IIP3) is 3.5 dB at 7 GHz to prove the linear behavior of the proposed LNA. The simulation of this circuit can achieve more than 23dB of attenuation at 5.3 GHZ and consumes 7.8mW. Thus, the proposed LNA is Suitable for low power and robust wireless UWB applications.

Keywords: UWB LNA, notch filter, current reuse, noise figure, robust, linear

I. INTRODUCTION

Since 2002, the Federal Communications Commission (FCC) has authorized the use of the ultra-wideband (UWB) technology to deal with the requirement of today's communication systems. The ultra- wideband is a radio technology, which occupies a large spectrum from 3.1 to 10.6 GHZ with a limited energy level settled at -41 dBm/MHZ to coexist with other existing standards. In fact, Ultra-wideband (UWB) systems allow high data rate for short range communication and low power consumption, which are suitable for various fields such as: Wireless personal area network, medical image systems, digital cameras and cellular phones. However, the existing wireless LANs standard (WLANS) overlaps with this UWB protocol over the band 5-6 GHZ and 2.4 GHZ [2]. Regarding the high level of the interference which exceeds the received ultra wideband signal by more than 60 dB, the UWB receiver chain will be affected. These interferes are shown in Figure 1. It induces a damaging effect on the received signal by causing gain compression and intermodulation products. To cancel these interferences, UWB systems can employ the Orthogonal Frequency Division Multiplexing (OFDM) technique which is based on using several narrowband subcarriers. Thus, OFDM appears as a promising candidate that suppresses the inter-symbol interferences, enhances the spectral efficiency and the data rate of wireless communication systems [15-16].

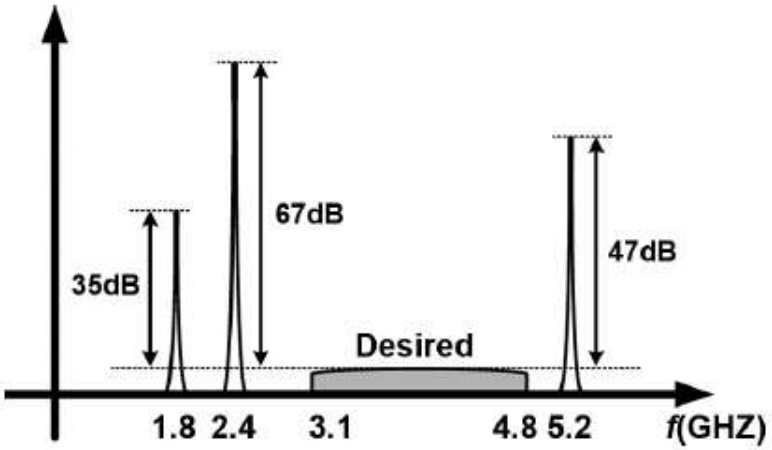


Figure.1. Spectrum of UWB system with inerference.

Because the UWB LNA is the first block in UWB receiver, is responsible to establish the general system sensitivity. Hence, to overcome this issue these interferences should be attenuated by integrating a notch filter with the UWB LNA. In order to obtain high performance of the receiver chain, a clear specification of the notch filter is summarized in Table1.

Table 1. Specification of the Notch filter.

Standard	Notch center freq (GHZ)	10dB attenuation bandwidth	Peak attenuation(dB)
GSM-1800/1900	1.85	1.7~199	
802.11b/g	2.44	2.4~2.48	
802.11a	5.25	5.15~5.35	>20

On the other hand, there are various topologies for designing wideband low noise amplifiers principally incorporate, resistive shunt-feedback topology [3], the distributed configuration [9], common-gate termination [10], and LC input network [11]. Recently, academic research has developed an innovative structure of the wideband amplifier which incorporates a notch filter with negative resistance [12] in order to achieve a deep out-band rejection.

This paper focuses on the design of an UWB LNA which fulfills the desired requirements with an active notch filter and is organized as follows. After a brief introduction to the architecture of ulra-wideband LNA with a theoretical analysis of the notch filter and its optimization given in Section II. Section III, shows the experimental results. Finally, conclusion is drawn in Section IV.

II. ANALYSIS AND DESIGN OF THE PROPOSED DUAL WIDEBAND LNA

A. Dual wideband LNA design

As shown in Figure 2, the proposed LNA is a cascode stage forming by two common source amplifiers (M1, M2). Obviously, the cascode structure increases the gain thanks to its high output impedance, suppress the Miller effect and establish good isolation [10]. Moreover, the design incorporates the resistive-current reuse technique which reduces the power consumption. One of the essential challenges in designing this UWB LNA is to ensure a good rejection of the interference covering the band 5-6 GHZ range. However, there is a trade-off between the wideband input

matching and out-band rejection. Hence, optimum design should establish both weak interfers and wideband input matching. In the design, the input RF signal is received by the input pad RFin and is delivered to the first transistor M1 in order to be amplified. The series resonant circuit consisting of the capacitor Cin and the inductor L in and the degeneration is used to establish the input wideband matching impedance. Moreover, Cin which has the value of 2pf is used as a DC blocking capacitor. Also, a degeneration inductor Ls which is placed in series with source enhances the stability of the design and should be small of 0.236nH. Moreover, the PMOS transistor Mp coupled with the resistor Rb1 are used to bias the transistor (M1) in class AB in order to ensure more linearity. On top of that, the resistive-feedback technique is established by the two stage amplifier (M1, M2) thanks to the resistive-capacitive shunt feedback. After being amplified by transistor M1, the output signal will be forwarded to the gate of transistor M2.So, this current-reuse core leads immediately to share the same bias voltage between the two transistors (M1, M2). Moreover, the two inductor load (L1, Ld) furnish a high impedance path to authorize the DC source to flow through and the drop of voltage among them was negligible. Assuming a drain current of 7.8mA to be drawn by transistor M1, the calculated size for NMOS transistor M1 is approwimately 116 µm under saturation [10]:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L}(V_{GS1} - V_{tn})^2 \quad (1)$$

Where Cox = εox/Tox =8.6E-3Pf/μm^2 , Vgs1=0.75V (class AB operation), Vt = 0.5 V, $\mu_n C_{ox} = 387(\mu A/V^2)$ for a typical 0.18µm CMOS-process.

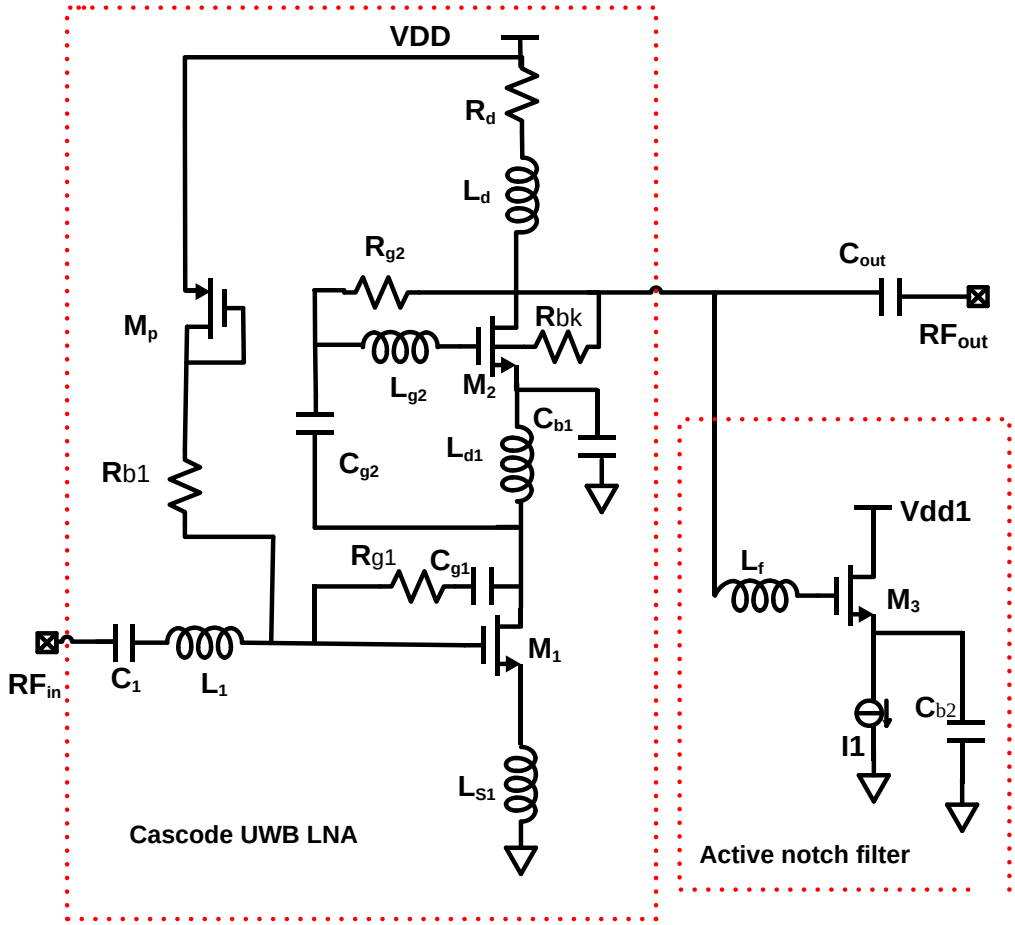


Figure 2. Schematic of the proposed dual wideband CMOS LNA.

Ld1 is connected between the two transistors in order to widen the bandwidth of frequency range. A series peaking inductive load Lg2 is connected to the gate of M2 to double the 3dB bandwidth of the output stage. To implement further minimum power consumption, the forward body biasing technique is applied to transistor M2 in order to decrease the threshold voltage Where, the body bias terminal is joining the drain pad of the transistor M2 using a current limiting resistor Rbk. Cb1 and Cb2 are the bypass capacitor to suppress the high frequency noise from the power supply. Finally, the capacitor Cout is playing the role of the output impedance matching circuit.

B. Input wideband matching impedance

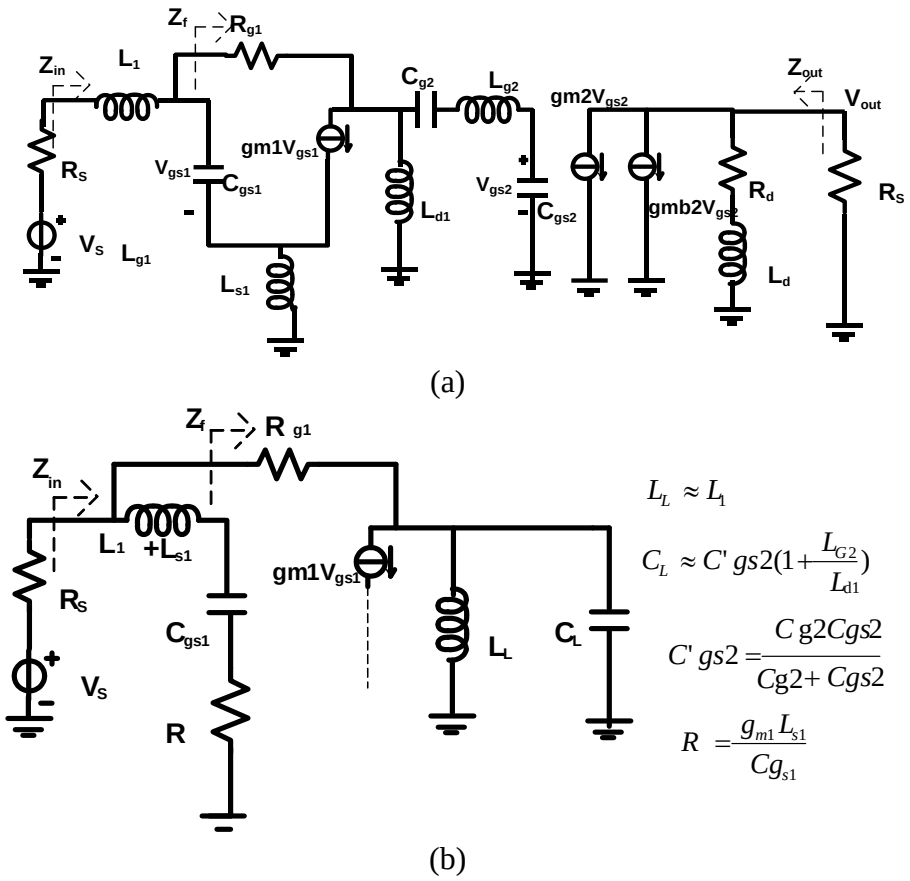


Figure 3. (a) Schematic of the proposed wideband CMOS LNA. (b) Simplified small signal equivalent circuit.

Achieving a wideband input matching is a relevant task. The used technique is to adopt the traditional technique which employs a source degeneration inductor with the resistive feedback topology to ensure acceptable input impedance matching and minimum noise over the desired bandwidth. Our goal is to conjugate match the input port of the circuit to the signal source output impedance Rs at a certain resonance frequency ωo. Figure 3 (a) and (b) display the schematic and simplified small-signal equivalent circuit of the proposed ultra wideband LNA. Thus, the input impedance can be written as follows:

$$Zin = Z_{in1} // Z_f = \left[s(L_S) + \frac{1}{S_{cgs1}} + \frac{(g_{m1})}{cgs_1} L_S \right] // Z_f \quad (2)$$

Zin1 introduces the input impedance of LNA neglecting the effect of the shunt feedback branch (RF), where gm1 and cgs are the transconductance and the gate source capacitor of transistor M1. However, Zf is the equivalent input impedance looking into the resistive-shunt feedback, and it can be represented as below:

$$Z_f = \frac{R_F + \left(sL_L // \frac{1}{Sc_L} \right)}{1 + \frac{g_{m1}}{s^2 C_{gs1}(L_{g1} + L_S) + s(g_{m1})L_S + 1} \cdot \left(sL_L // \frac{1}{Sc_L} \right)}$$

At the low cut-off frequency, some assumptions are taken:

$$SL_L // \frac{1}{ScL} \succ\succ 1$$

$$S^2 c_{gs1}(L_1 + L_{S1}) + Sg_{m1}L_{S1} \prec\prec 1$$

Hence, the input impedance will be equivalent to Zf and is defined from (3) as below:

$$Z_{in} \approx Z_f = S\left(\frac{R_F C_L}{g_{m1}} \right) + \frac{1}{S\left(g_{m1} L_{L/R_F} \right)} + \frac{1}{g_{m1}} \quad (4)$$

At high resonance frequency, the input impedance and the resonance frequency are given below:

$$Zin \approx Zin_1 = \left[S(L_1 + L_{S1}) + \frac{1}{S_{cgs1}} + W_{T1}L_{S1} \right] \quad (5)$$

Using the conjugate matching, the high resonance frequency is determined from (5) and expressed as below:

$$W_H = \frac{1}{\sqrt{(L_1 + L_{S1})C_{gs1}}} \quad (6)$$

Where $Cgs = \frac{2}{3} Cox.W.L_{\min}$

And Cox = εox/Tox =9.46E-3Pf/μm^2 for a typical 0.18μm CMOS-process. Thus, this gate capacitance has the value of 131.683e-3pF for the transistor M1 which has the width 110μm. From (6), the calculated resonance frequency is approximately 11.57 GHZ for the typical values of L1and LS1 are 1.2nH, 0.236nH. The same process is used to determine the low cut-off frequency $F_L = \frac{\omega_H}{2\pi}$

Combining the two resonance frequencies will establish the wide bandwidth.

C. Active notch filter

Recent research focus on designing LNA with notch filter to ensure robust wireless communication systems [6-7]. Figure 4 (a) and (b) show the circuit design of the second order active notch filter and its simplified small signal equivalent. From Figure 4(b) the input impedance of the filter is given by [18]:

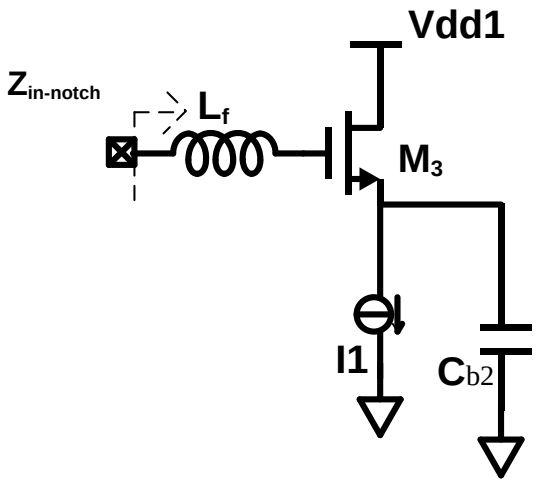
$$Z_{\text{in-notch}} = j\omega L_f + \frac{1}{j\omega}\left(\frac{1}{C_{gs3}} + \frac{1}{C_{b2}}\right) - \frac{g_{m3}}{\omega^2 C_{gs3} C_{b2}} + R_{Lf} + r_{g3} \quad (7)$$

Where Cgs3, gm3, rg3 are the gate–source capacitor, transconductance, series gate resistance of transistor M1, and Rlf is the series resistor load of inductor Lf.

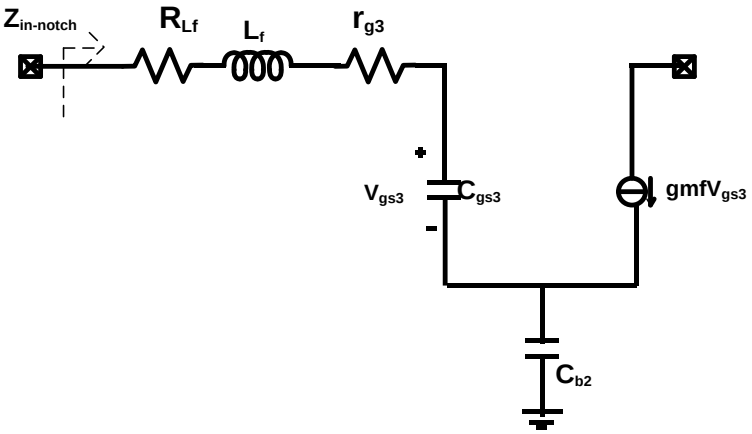
The negative term appears on (7) corresponds to the negative resistance seen at the gate of transistor M3. To cancel all the parasitic items, it should maintain only the imaginary part of the impedance. It leads to a suitable adjustment of the bias current I1 to vary the transductions gm3 which neglects the effect of the series resistances RL1 and rg3. In fact, the input impedance will be expressed as below:

$$Z_{in\text{-}notch} = \frac{s^2 L_f C_{eq} + 1}{sC_{eq}} \quad (8)$$

Where $C_{eq} = \frac{1}{C_{b2}} + \frac{1}{C_{gs3}}$



(a)



(b)

Figure 4. (a) Schematic of the second order active notch filter. (b) Simplified small signal equivalent circuit.

When the impedance Znotch considering the filter is diminished, the undesired signal will be extracted from the original path to ground. Thus, a deep rejection at this undesired frequency is established. This frequency is noted fnotch and is determined from equation (9) as below:

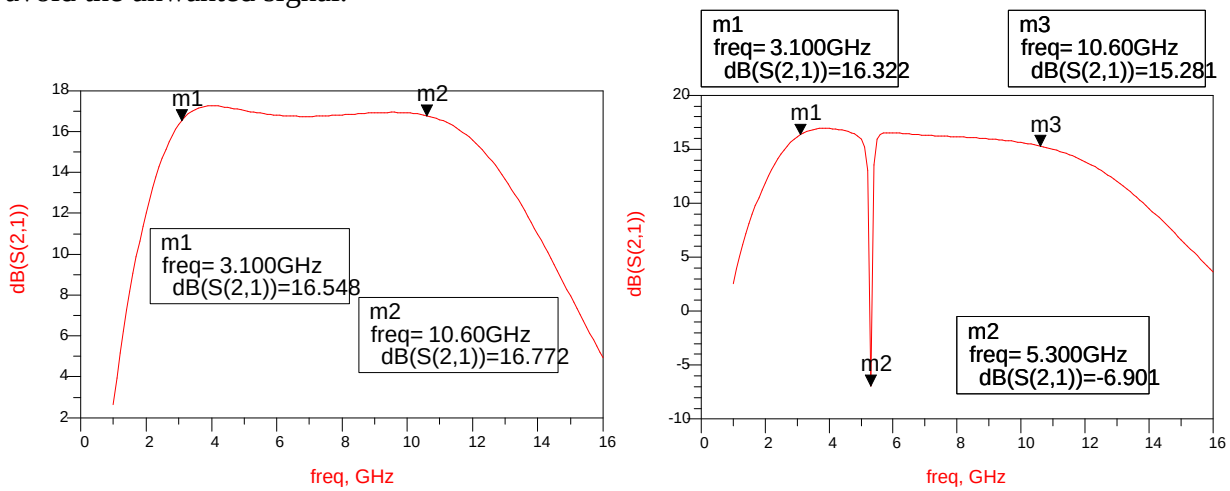
$$f_{notch} = \frac{1}{2\Pi\sqrt{L_f C_{eq}}} \quad (9)$$

III. RESULTS AND DISCUSSIONS

The proposed UWB LNA circuit integrating an active notch filter and spanning the frequency band 3.1-10.6 GHZ is simulated using Agilent Advanced Design System (ADS) using TSMC CMOS 0.18µm technology. The simulation results are disclosed below.

A. Gain analysis

As can be seen in Figure 5. (a), the simulated gain (S21) of the proposed LNA without active notch filter has a high and flat gain of 16dB from 3.1 to 10.6 GHZ .Besides, Figure 5. (b) shows the simulated gain of the UWB LNA integrating the active notch filter. It is observed at 5 .2 GHZ, there is a deep increase in the simulated (S21) due to the minimum value of the input impedance Zin of the notch filter at this resonnance frequency. Hence, the power gain of the LNA will be degraded to avoid the unwanted signal.



(a) (b)

Figure 5. Simulated power gain (S21) of the LNA : (a) without filter, (b) with filter.

B. Input, output matching impedance and reverse isolation.

Figure 6 shows the simulated input reflection coefficient (S11) which is well down to -9.6 dB for the entire operating frequencies. As explained before, the input matching of the LNA is set by choosing the optimum input matching network and using the current reuse core.

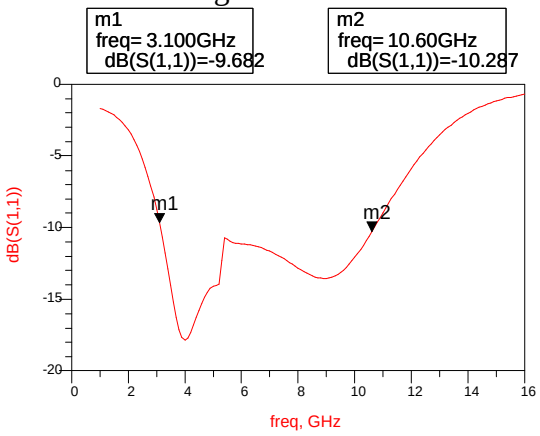
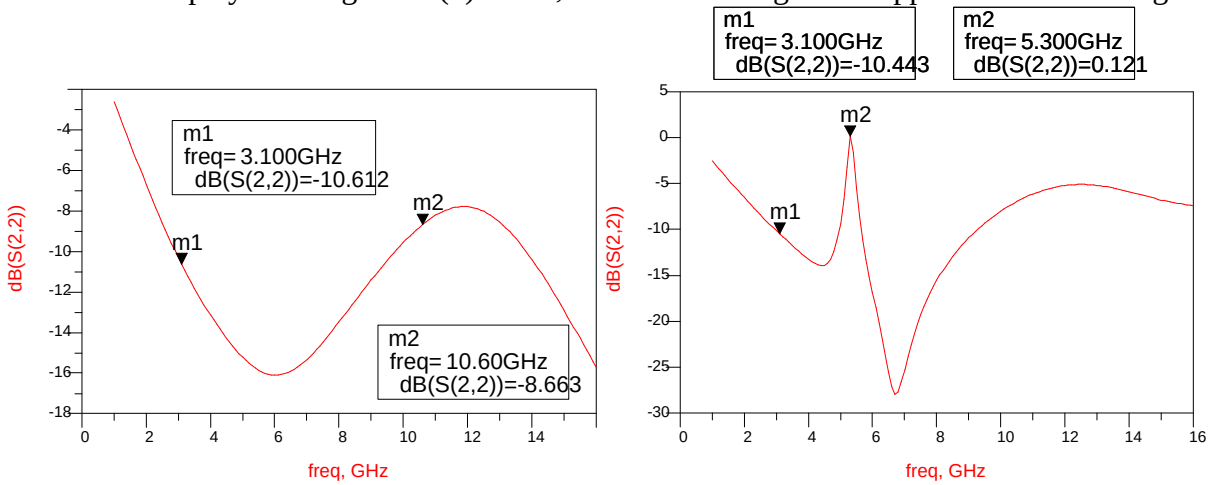


Figure 6. Simulated input return loss vs frequency.

About the output matching impedance (S22), it was a sharp increase until reaching 0 dB at frequency 5.3GHZ as displayed in Figure 7. (b). Thus, the unwanted signal is suppressed from the signal path.



(a) (b)

Figure 7. Simulated output return loss (S22): (a) without filter, (b) with filter.

As can be seen in Figure 8, the reverse isolation metric establish a perfect value less than -30 dB over this bandwidth to enhance the isolation between output terminal and input terminal. Using the bypass capacitor (Cb) between the two stage amplifiers (M1, M2) and incorporating a peak inductor (Ld2) enhance this metric.

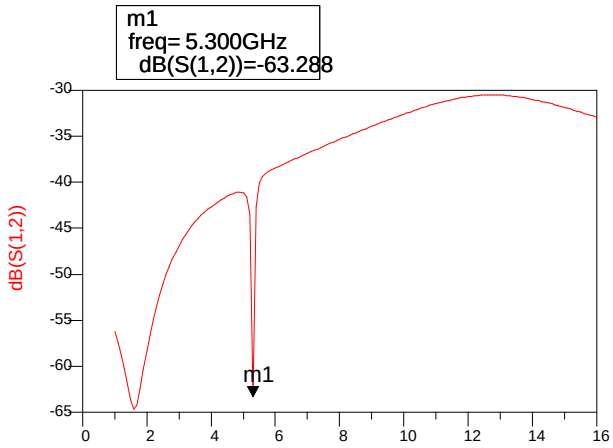
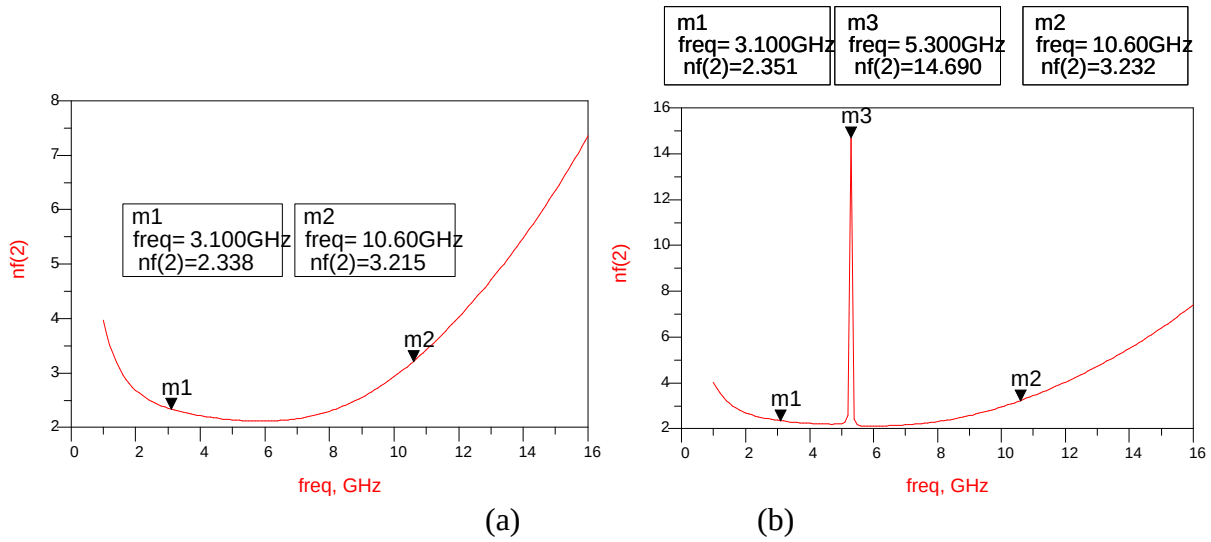


Figure 8. Simulated reverse isolation (S12)vs frequency

C. Noise figure

Figure 9. (a) shows the term NF which is within 2.3–3.2 dB over the entire band 3.1-10.6 GHz without incorporating the notch filter thanks to the resistive feedback topology. However, the use of the active notch filter induces a rise in the interference region due to the resistive character of Q-enhanced filter circuit.



(a) (b)

Figure 9. Simulated noise figure vs frequency: (a) without filter, (b) with filter.

D. Linearity

Linearity is a relevant metric to characterize the performance of the LNA. It can limit the transmission of the effective power to the load. The commonly used parameter to define the linearity is the the third-order intercept point (IIP3). Figure 10 discloses an IIP3 about 3.5 dB for input power of -10dbm and frequency 7GHZ.

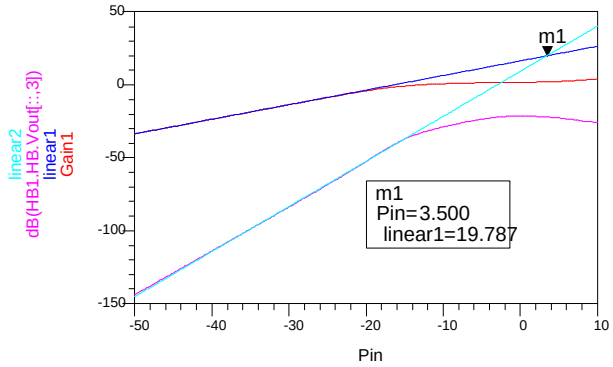


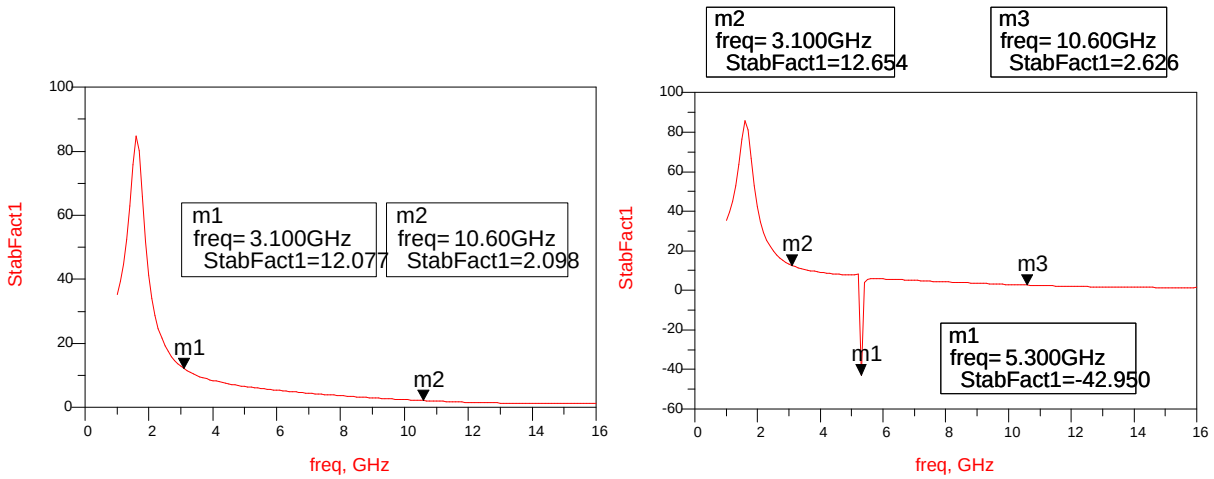
Figure 10. Simulated IIP3 vs frequency.

E. Stability analysis

Stability factor (K-factor) is another focus in designing the LNA. To ensure the stability of this design, it should satisfy the following expression below:

$$K_f = 1 + \frac{|\beta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{12}|} > 1 \quad (10)$$

From figure 11. (a), the LNA complies with the condition and is is unconditionally stable over the allotted band from 3.1 to 10.6GHZ. Whereas, in Figure 11. (b), it was a clear decrease in the interference region (5.3 GHZ) to ensure that the LNA is not unconditionally stable due to the effect of the notch filter to dismiss this frequency.



(a) (b)

Figure 11. Simulated stability Kf vs frequency: (a) without filter, (b) with filter.

Table 2 presents the high performance of the proposed dual- Wide-Band LNA and makes comparison with the previously reported LNA incorporating a notch filter. The great features furnished are a deep out-band rejection in the interference region, high and flat gain, low noise and high linearity.

Table 2. The proposed LNA features comparison

Ref	CMOS technology	Frequency (GHZ)	Gain (dB)	S11 (dB)	S22 (dB)	Nf (dB)	IIP3 (dB)	Rejection Gain(dB)	Year
This work	0.18	3.1-10.6	16±0.8	<-9.6	<-10	2.3-3.2	3.5	23.8@5.3GHZ	2017
[3]	0.18	3.1-10.6	15	<-10	N/A	<2	N/A	>28@5.5GHZ	2016
[4]	0.18	0.8-1.7	13-17.5	<-18	N/A	2.17-3.4	7.36	N/A	2016
[5]	0.18	3.2-6.3	14.96	<-10	N/A	0.95	N/A	94@6.3GHZ	2015
[6]	0.18	3.1-10.6	18.7-10	<-10	<-11	4.8	-8.1	>20@4.75GHZ	2013
[14]	0.18	2.9-4.9	13.2	<-4	N/A	3.9	N/A	42@1.9GHZ 66@8.5GHZ	2012
[7]	0.18	1.2-9.5	14.7	<-10	<-10	5.3	-2.5	35.7@5.5GHZ	2011
[8]	0.18	3.1-10.6	16-18	<-7	<-10	3.5	N/A	>25@5.6GHZ	2011

N/A: not mention

IV. CONCLUSION

This paper presents circuit LNA with interference rejection using 0.18 m CMOS technology. The proposed cascode structure employs the current-reuse core and resistance-feedback technology to ensure wideband input matching with low power consumption and minimum noise. An active notch filter is used to ensure the robustness to in-band interferences. It achieves a deep out-band rejection more than 20 dB over the WLAN band at 5.3 GHZ. From 3.1 to 10.6 GHz, the power gain is higher than 15 dB and the minimum noise figure is 2.7 dB. IIP3 is 3.5 dB to ensure the high linearity of the proposed LNA. Thus, the great features make the LNA suitable for robust wireless UWB communication systems.

Conflict of interest: The authors declare that they have no conflict of interest.

Ethical statement: The authors declare that they have followed ethical responsibilities.

REFERENCES

[1] Stroh, S. (2003).Ultra-wideband: multimedia unplugged. IEEE Spectr., 2003, 40, (9), pp. 23–27.
J. Clerk Maxwell (1892). A Treatise on Electricity and Magnetism. 3rd ed., vol. 2. Oxford: Clarendon, pp.68–73.

[2] S. Lo, I. Sever, S.-P. Ma, P. Jang, A. Zou, C. Arnott, K. Ghatak, A. Schwartz, L. Huynh, V. T. Phan, and T. Nguyen (2007). A dual-antenna phased-array UWB transceiver in 0.18-µm CMOS. IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2776–2786, DOI: 10.1109/JSSC.2006.884803·

[3] Nasrullah Saifullah 1, Zahriladha Zakaria 1, Azahari Salleh 1 , Siti Rosmaniza Ab Rashid 1 , Anthony Bruster (2016). Integrated Low Noise Amplifier with Notch Filter Using DMS Technique for Ultra-wideband Application. 2016 3rd International Conference on Electronic Design (ICED), August 11-12, 2016, Phuket, Thailand, DOI: 10.1109/ICED.2016.7804606.

[4] Jhen-Ji Wanga, Duan-Yu Chen et al (2016). A multi-band low noise amplifier with wide-band interference rejection improvement. International Journal of Electronics and Communications (AEÜ), Int. J. Electron. Commun. (AEÜ) 70 (2016) 320–325, DOI: 10.1016/j.aeue.2015.12.010.

[5] M. Ikram Malek , Suman Saini (2015). Improved Two Stage Ultra-Wideband CMOS Low Noise Amplifier with Out Band Rejection Using Low Noise Active Inductor. SPACES-2015, Dept of ECE, KL UNIVERSITY, DOI: 10.1109/SPACES.2015.7058237.

[6] Meng-Ting Hsu, Po-Yu Lee, Yu-Zhang Huang (2013). Design of Dual-Wideband Low Noise Amplifier base on Common Gate Topology. ASIC (ASICON), 2013 IEEE 10th International Conference.

[7] Jui-Yi Lin and Hwann-Kaeo Chio (2011). Power-Constrained Third-Order Active Notch Filter Applied in IR-LNA for UWB Standards. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 58, NO. 1, JANUARY 2011, DOI: 10.1109/TCSII.2010.2092825

[8] Nischal Koirala, R. K. Pokharel, A.I.A. Galal (2011). Design of a Low Noise Amplifier with Integrated Notch Filter for Interference Rejection in Ultra- Wideband Systems. CJMW2011 Proceedings.

[9] P. Heydari (2007). Design and analysis of a performance-optimized CMOS UWB distributed LNA. IEEE Journal of Solid-State Circuits, vol. 42, no. 9,pp. 1892–1905, Sep. 2007.

[10] Lee, T. H (2004). The Design of CMOS Radio-frequency Integrated Circuits. 2nd edition, Cambridge Univ. Press, Cambridge, UK,2004.

[11] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto (2006). A 0.18-µmCMOS selective receiver front-end for UWB applications. IEEE J. Solid-State Circuits, vol. 41, no. 8, pp. 1764–1771, Aug. 2006.

[12] A. Bevilacqua and A. M. Niknejad (2004). An ultra wideband CMOS lownoise amplifier for 3.1–10.6-GHz wireless receivers. IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[13] A. Bevilacqua, A. Vallese, C. Sandner, M. Tiebout, A. Gerosa, and A.Neviani (2007). A 0.13-µm CMOS LNA with integrated balun and notch filter for 3 to 5 GHz UWB receivers. in IEEE Int. Solid-State Circuits Conf. Tech. Dig., Feb. 2007, pp. 420–421, DOI: 10.1109/ISSCC.2007.373473.

[14] R.S.Sai Ram, Dr.T.Madhu, P.Lakshmi Sarojini (2012). Analysis and Design of CMOS Cascode LNA for UWB Applications with Gain Enhancement and Out- Band Rejection Capability. International Journal of Engineering Research & Technology (IJERT).

[15] A.S. Khan, A.H. Fauzi, R. Thangaveloo, A.A. Julahi, S. Tarmizi, A Review on Orthogonal Frequency Division Multiple Access (OFDMA) in Broadband Wireless Access, International Journal of Advanced Engineering Research and Applications (IJAERA), Volume – 1, Issue – 8, December – 2015.

[16] A.S. Khan, A.H. Fauzi, R. Thangaveloo, A.A. Julahi, S. Tarmizi, OFDM: A potential Candidate for 5G Networks, International Journal of Advanced Engineering Research and Applications (IJAERA), Volume – 1, Issue – 7, November – 2015.

